ADS-STANDALONE/9R1
User Manual

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1 Introduction

The ADS-STANDALONE/9R1 is a stand-alone RFSoC enclosure providing 16-RF analogue channels, Ethernet, RS232 Serial COM, USB, and QSFP IO. The RF channels can run up to 10GSPS (DAC) and 5 GSPS(ADC)

The ADS-STANDALONE/9R1 uses a single 15V-30V input power supply. An on-board system monitor micro-controller provides voltage/current monitoring of the generated power supplies, as well as providing the capability to turn the supplies on/off via the micro USB interface. A USB to JTAG circuit is also provided, giving access to the JTAG chain without requiring an external JTAG box.

1.1 Key Features

Key Features

- Xilinx RFSoC FPGA with PS block consisting of:
  - Quad-core ARM Cortex-A53, Dual-core ARM Cortex-R5, Mali-400 GPU
  - 1 bank of DDR4-2400 SDRAM 2GB
  - Two Quad SPI Flash memory, 512Mb each
  - USB
  - RS232 serial COM port
  - Gigabit Ethernet
- Programmable Logic (PL) block consisting of:
  - 4 HSSIO links to the QSFP connector
  - 2 banks of DDR4-2400 SDRAM, 1GB per bank
- RF Sampling block consisting of:
  - 8 12-bit 4/5GSPS RF-ADCs
  - 8 14-bit 6.5/10GSPS RF-DACs
  - 8 soft-decision FECs (ZU28DR/ZU48DR only)
  - Full Scale Input (100MHz/ZU27DR): 5.0dBm
  - Full Scale Output (100MHz/20mA Mode/ZU27DR): -4.5dBm
  - Full Scale Output (100MHz/32mA Mode/ZU48DR): 1.15dBm
- Front Panel IO Interface with:
  - 8 HF single ended ADC signals
  - 8 HF single ended DAC signals
  - Reference clock input for the RF sampling blocks
  - Reference clock output from RF sampling blocks
  - 2 digital GPIO

Figure 1 : ADS-STANDALONE/9R1

ADMC-XMC-STANDALONE User Manual: https://www.alpha-data.com/xml/user_manuals/adc-xmc-standalone%20user%20manual.pdf

ADM-XRC-9R1 User Manual: https://www.alpha-data.com/xml/user_manuals/adm-xrc-9r1%20user%20manual.pdf

ADM-XRC-9R1 Reference Design: https://www.alpha-data.com/resource/admxrc9r1

2 Main Input Power Supply Requirements

The total power requirement will vary depending on the particular FPGA design. A 60W supply would likely be more than enough for most FPGA designs before thermal limits of the device and heatsink become the limiting factor. Alpha-Data can provide a power supply estimator spreadsheet to estimate the total power requirements for a particular FPGA design. An example compatible power supple is RS PRO part number 175-3290: https://uk.rs-online.com/web/p/ac-dc-adapters/1753290

Spec	Value
Voltage	15V-30V
Power	60W
Current	5A Max.
Connector	2.1mm x 5.5mm DC power plug, centre pin positive

Table 1 : Suggested Input Supply Specifications

3 Installation and Power Up

1) Connect a serial cable to the serial port and connect the other end to a USB-to-serial converter.

2) Open a serial terminal with at 115200 baud, 8 data bits, 1 stop bit.

3) Turn the power switch on, and the PS should start to boot from then internal SD card.

4) Once booted login with the username "root" and password "root"

5) To run the RF example design, use the command "boardtest-9r1"

See the example design user guide for details on the operation of the boardtest-9r1 application

4 JTAG Interface

A USB to JTAG circuit is provided, giving access to the XMC JTAG interface without the need for an external programming box (e.g. Xilinx Platform Cable II). The USB to JTAG converter is compatible with Vivado, and will appear in hardware manager as a Digilent device. A 14-pin JTAG header is also available, with an on-board multiplexer to switch between the 14-pin header or the USB to JTAG converter. The multiplexer selects the USB to JTAG circuit when a micro USB cable is attached.

5 Current/Voltage Monitoring

The ADS-STANDALONE/9R1 provides current sense functionality on the 12V and combined 3V3 internal supplies. These values can be reported over the micro-USB interface, using the alpha-data "avr2util" utility.

Avr2util for Windows and the associated USB driver can be downloaded here:
https://support.alpha-data.com/pub/firmware/utilities/windows/

Avr2util for Linux can be downloaded here:
https://support.alpha-data.com/pub/firmware/utilities/linux/

Use "avr2util.exe /?" to see all options.
For example "avr2util.exe /usbcom \\.\com4 display-sensors" will display all sensor values.

Note that 'com4' is used here as an example, and should be changed to match the com port number assigned under windows device manager

6 On-Board Generated Power Supplies

The ADS-STANDALONE/9R1 generates the 3V3/3V3_AUX/12V0/-12V0 supplies required by the XMC site from a single 15V-30V input supply. Each supply has the following specifications:

Power supply	Voltage (V)	Max. current (A)	Monitoring
3V3_DIG	3.3	7.0 [1]	Voltage and current [1]
3V3_AUX	3.3 [2]	7.0 [1]	Voltage and current [1]
12V0_DIG	12.0	7.0	Voltage and current

Table 2 : ADS-STANDALONE/9R1 Power Supplies

[1] The 3V3_DIG and 3V3_AUX rails are generated from the same supply, so the maximum current is the combination of 3V3_AUX + 3V3_DIG. The current monitoring also measures the combined current.

[2] The 3V3_AUX rail is an always-on 3.3V auxiliary power supply from the 15V-30V input.

The 3V3_DIG/3V3_AUX/12V0_DIG current usage of a particular design can be estimated using a power estimation spreadsheet. Contact support@alpha-data.com for access to the spreadsheet.

7 Front-Panel I/O

The front panel interface consists of a 20-way high-speed connector. This connector Supports an external reference clock input and output, two GPIO pins, 8 DAC signals and 8 ADC signals. The connector part number is Nicomatic CMM342D000F51-0020-240002.

Signal	Impedance (Ohms)	J2 pin number	Signal Level
ADC0	50	20	-
ADC1	50	19	-
ADC2	50	18	-
ADC3	50	17	-
ADC4	50	16	-
ADC5	50	15	-
ADC6	50	14	-
ADC7	50	13	-
DAC0	50	3	-
DAC1	50	4	-
DAC2	50	5	-
DAC3	50	6	-
DAC4	50	7	-
DAC5	50	8	-
DAC6	50	9	-
DAC7	50	10	-
REF IN	50	2	3.3V
REF OUT	50	1	3.3V
EXTIO0	-	12	3.3V
EXTIO1	-	11	3.3V

Table 3 : Front panel I/O signals

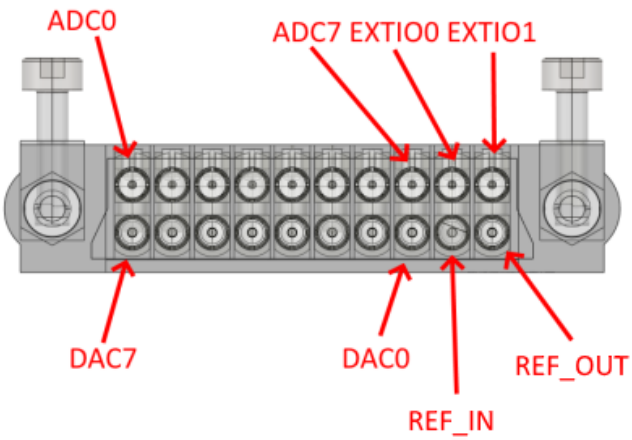

Figure 2 : Front Panel Pinout

8 Rear-Panel I/O

The rear panel interface consists of Power, USB, Ethernet, QSFP, RS-232 UART, 14-pin JTAG and micro USB connectors.

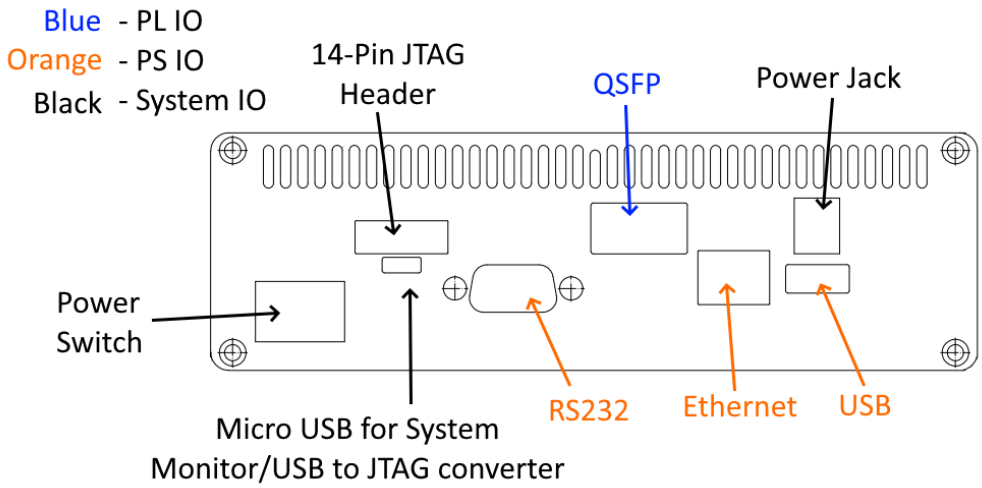

Figure 3 : Rear Panel Pinout

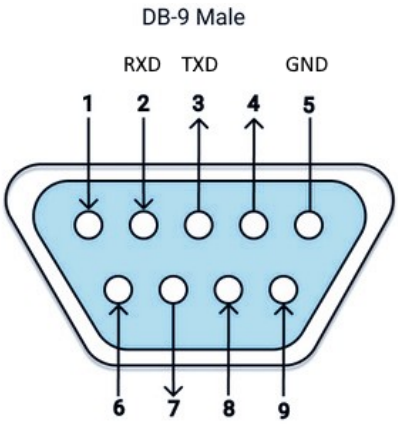

Figure 4 : RS-232 Pinout

9 QSFP pinout

The QSFP cage is connected to FPGA bank 129.

QSFP Lane	FPGA Bank 129 Lane
Tx0/Rx0	Tx3/Rx3
Tx1/Rx1	Tx2/Rx2
Tx2/Rx2	Tx1/Rx1
Tx3/Rx3	Tx0/Rx0

Table 4 : ADM-XRC-9R1 pcb revision 3+ pinout for J16

10 Dimensions

Dimension	Measurement
Width	170mm
Depth	235m
Height	67mm

Table 5 : ADS-STANDALONE/9R1 dimensions

11 Order Code

ADS-STANDALONE/X/T

Name	Symbol	Configurations
FPGA Card	X	9R1 = ADM-XRC-9R1

Table 6 : ADC-XMC-STANDALONE Order Code

Revision History

Date	Revision	Nature of Change
20 Oct 2022	1.0	First Release
27 Mar 2023	1.1	Added suggested part number for power supply, added IO diagram
15 May 2023	1.2	Added RS232 pinout

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